FIG. 1

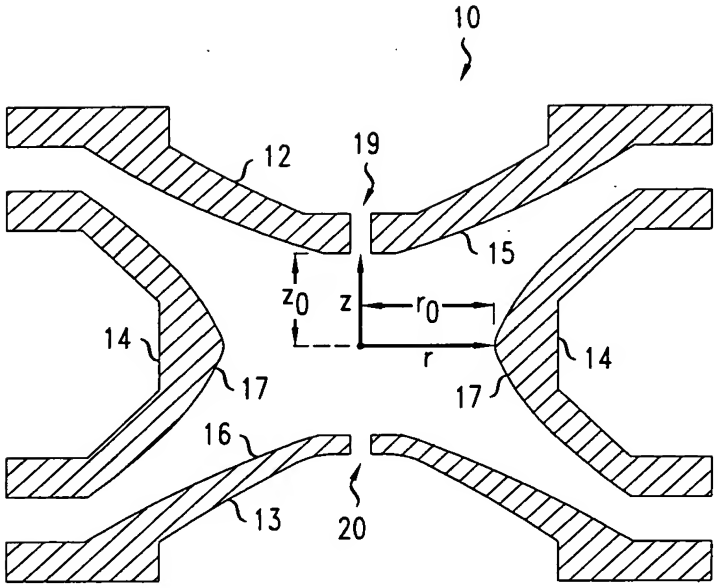


FIG. 2A

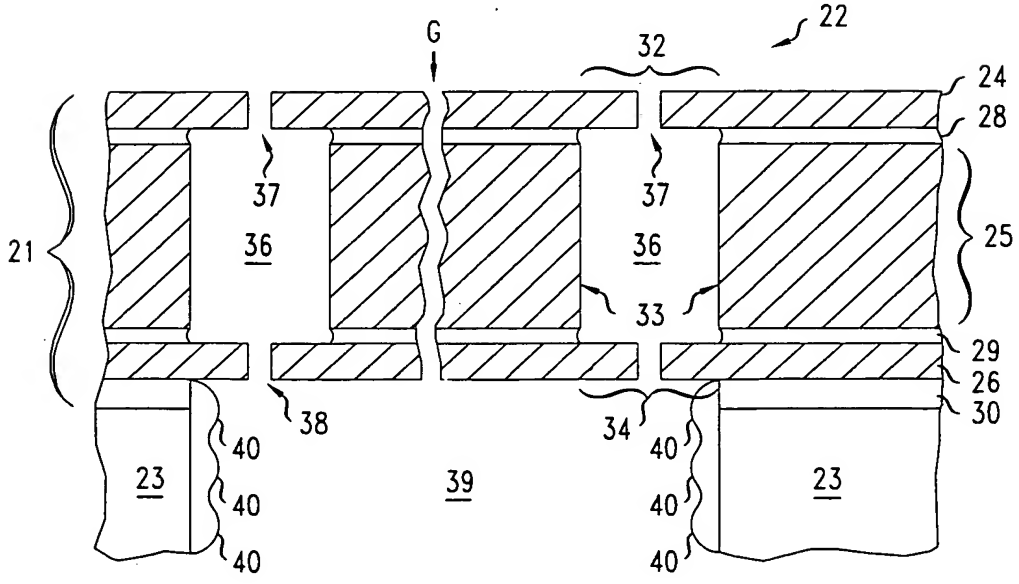


FIG. 2B

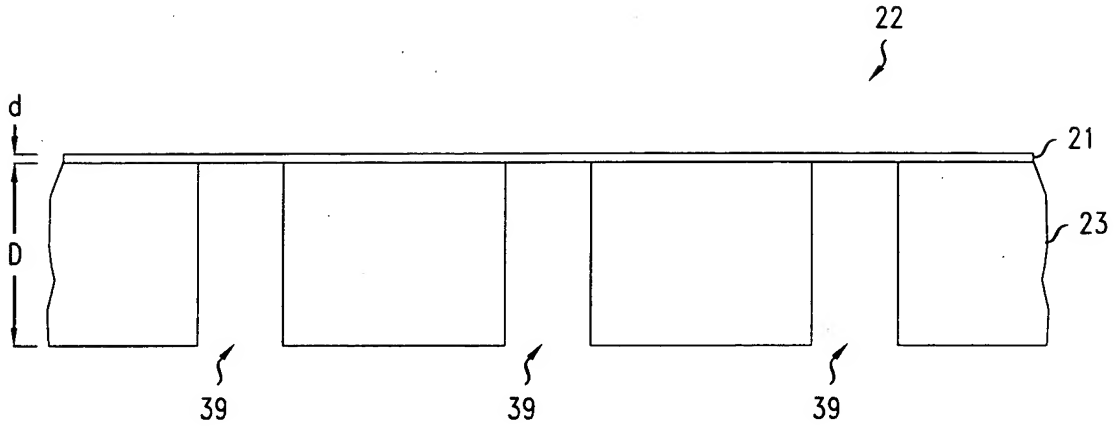


FIG. 2C

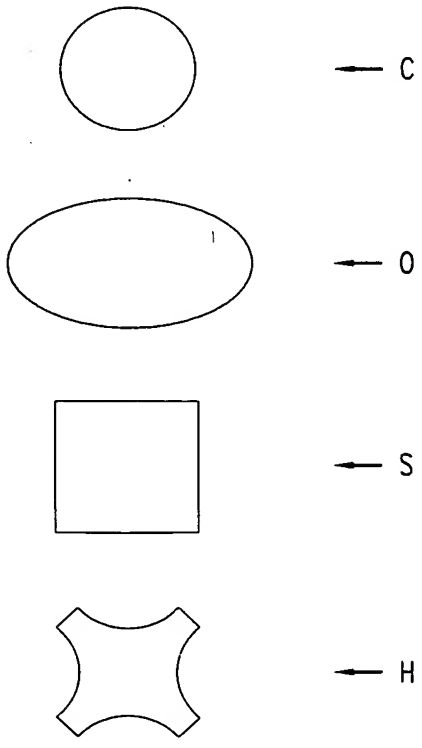
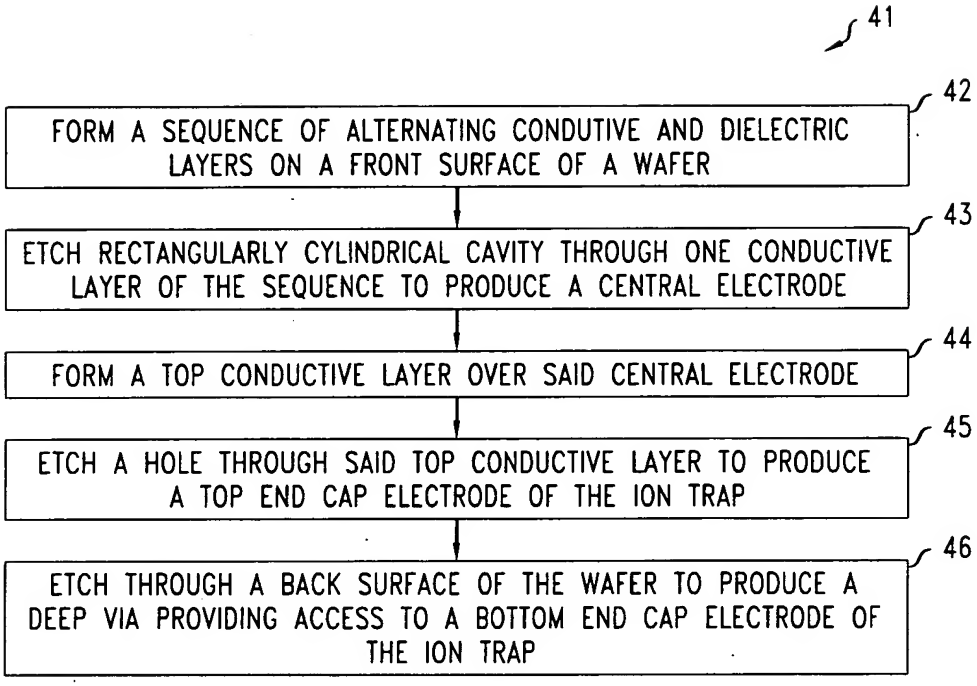


FIG. 3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FORM A SEQUENCE OF ALTERNATING CONDUTIVE AND DIELECTRIC LAYERS ON A FRONT SURFACE OF A WAFER
43
ETCH RECTANGULARLY CYLINDRICAL CAVITY THROUGH ONE CONDUCTIVE LAYER OF THE SEQUENCE TO PRODUCE A CENTRAL ELECTRODE
44
FORM A TOP CONDUCTIVE LAYER OVER SAID CENTRAL ELECTRODE
45
ETCH A HOLE THROUGH SAID TOP CONDUCTIVE LAYER TO PRODUCE A TOP END CAP ELECTRODE OF THE ION TRAP
46
ETCH THROUGH A BACK SURFACE OF THE WAFER TO PRODUCE A DEEP VIA PROVIDING ACCESS TO A BOTTOM END CAP ELECTRODE OF THE ION TRAP

FIG. 4

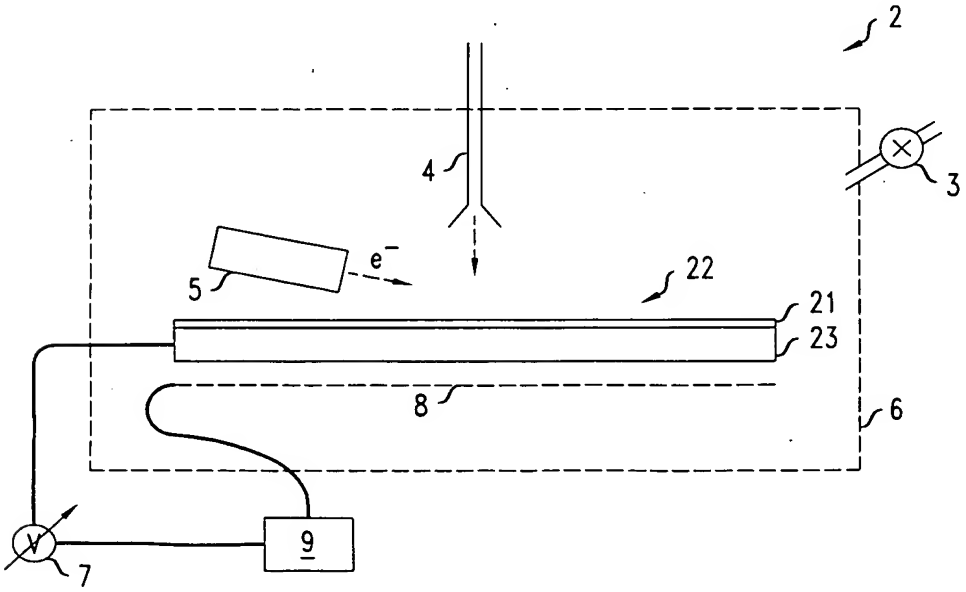
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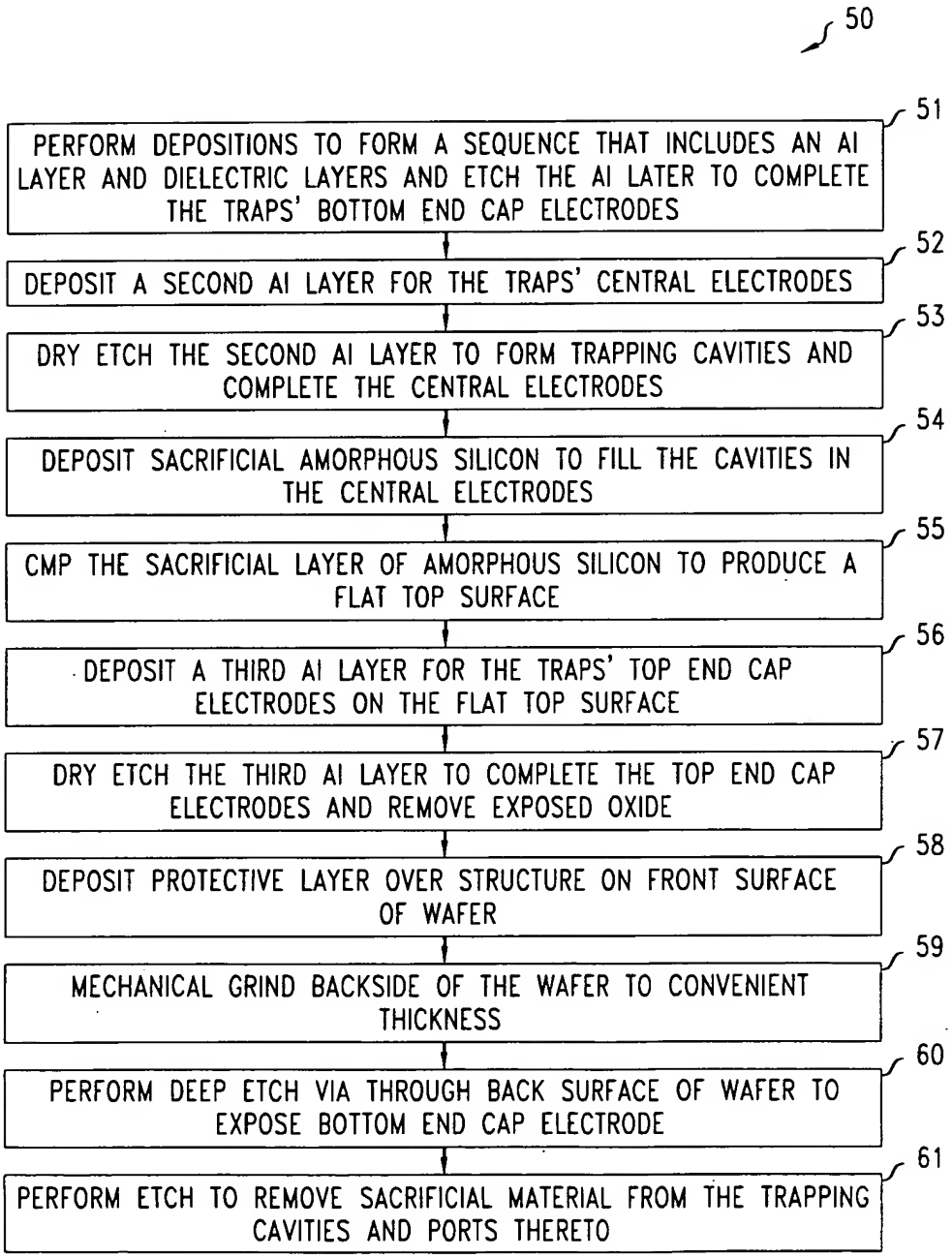
FIG. 5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PERFORM DEPOSITIONS TO FORM A SEQUENCE THAT INCLUDES AN Al LAYER AND DIELECTRIC LAYERS AND ETCH THE Al LATER TO COMPLETE THE TRAPS' BOTTOM END CAP ELECTRODES
51
DEPOSIT A SECOND Al LAYER FOR THE TRAPS' CENTRAL ELECTRODES
52
DRY ETCH THE SECOND Al LAYER TO FORM TRAPPING CAVITIES AND COMPLETE THE CENTRAL ELECTRODES
53
DEPOSIT SACRIFICIAL AMORPHOUS SILICON TO FILL THE CAVITIES IN THE CENTRAL ELECTRODES
54
CMP THE SACRIFICIAL LAYER OF AMORPHOUS SILICON TO PRODUCE A FLAT TOP SURFACE
55
DEPOSIT A THIRD Al LAYER FOR THE TRAPS' TOP END CAP ELECTRODES ON THE FLAT TOP SURFACE
56
DRY ETCH THE THIRD Al LAYER TO COMPLETE THE TOP END CAP ELECTRODES AND REMOVE EXPOSED OXIDE
57
DEPOSIT PROTECTIVE LAYER OVER STRUCTURE ON FRONT SURFACE OF WAFER
58
MECHANICAL GRIND BACKSIDE OF THE WAFER TO CONVENIENT THICKNESS
59
PERFORM DEEP ETCH VIA THROUGH BACK SURFACE OF WAFER TO EXPOSE BOTTOM END CAP ELECTRODE
60
PERFORM ETCH TO REMOVE SACRIFICIAL MATERIAL FROM THE TRAPPING CAVITIES AND PORTS THERETO
61

FIG. 6

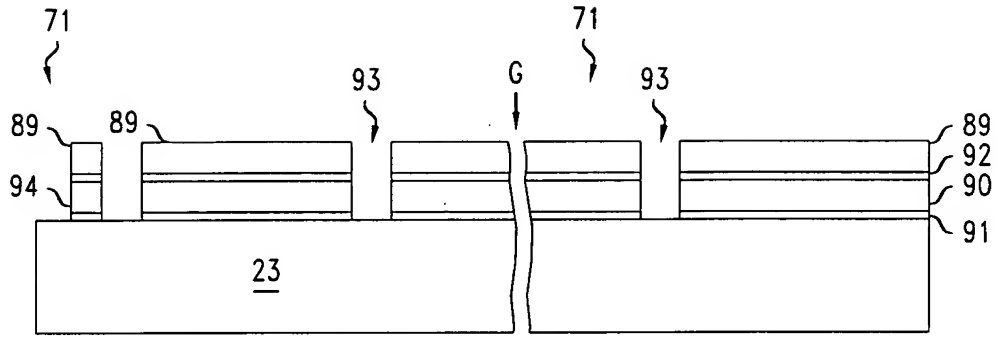

FIG. 7

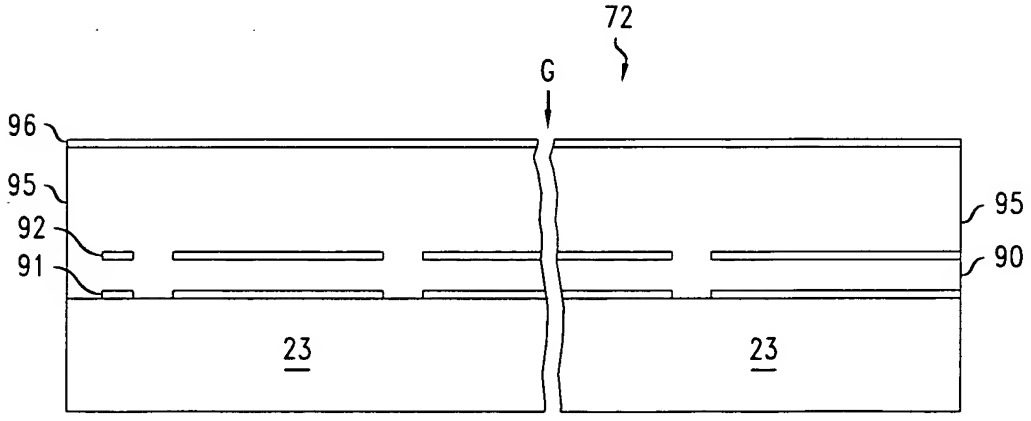

FIG. 8

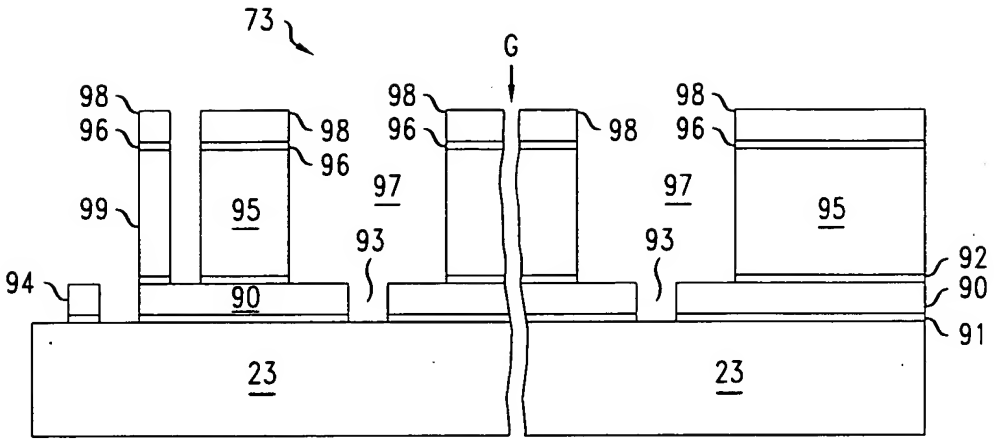
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FIG. 9

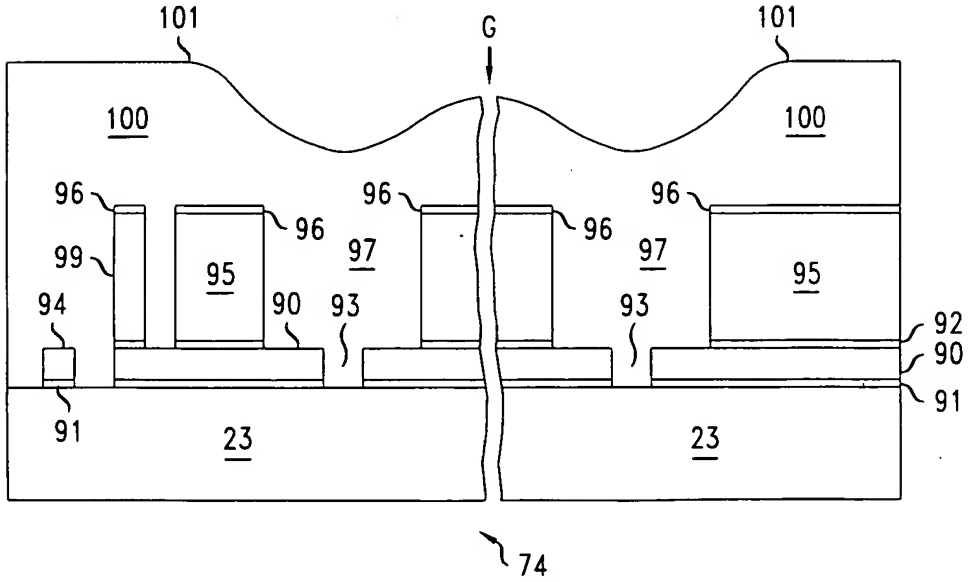
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FIG. 10

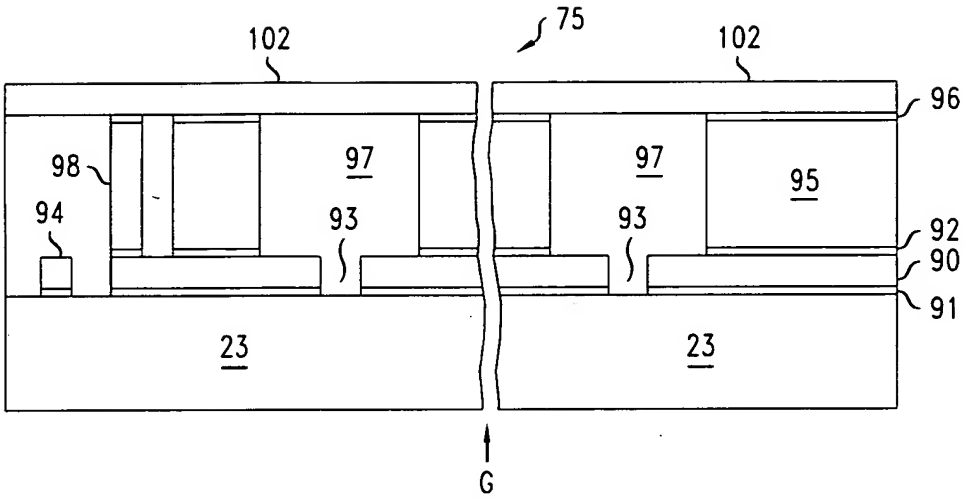
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FIG. 11

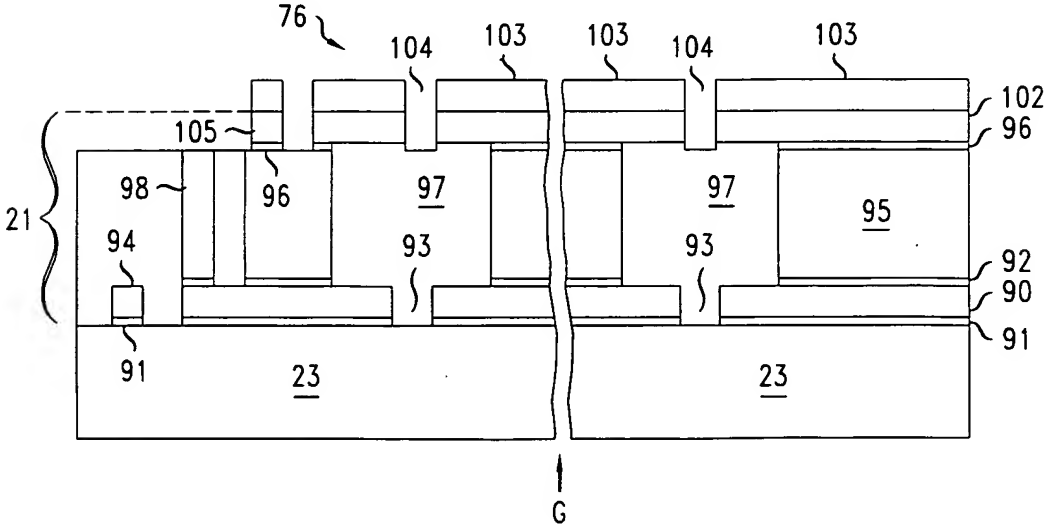
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FIG. 12

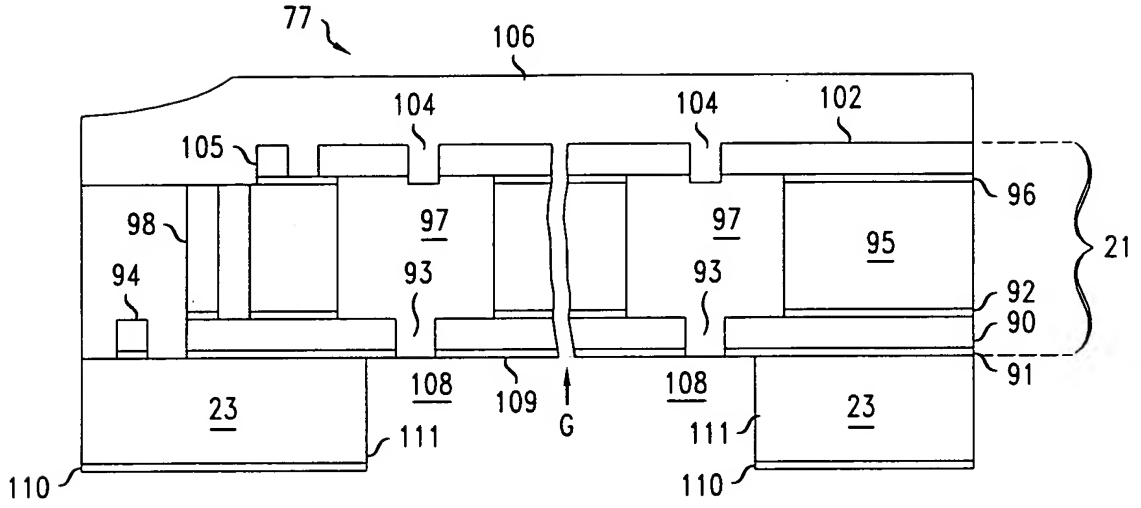
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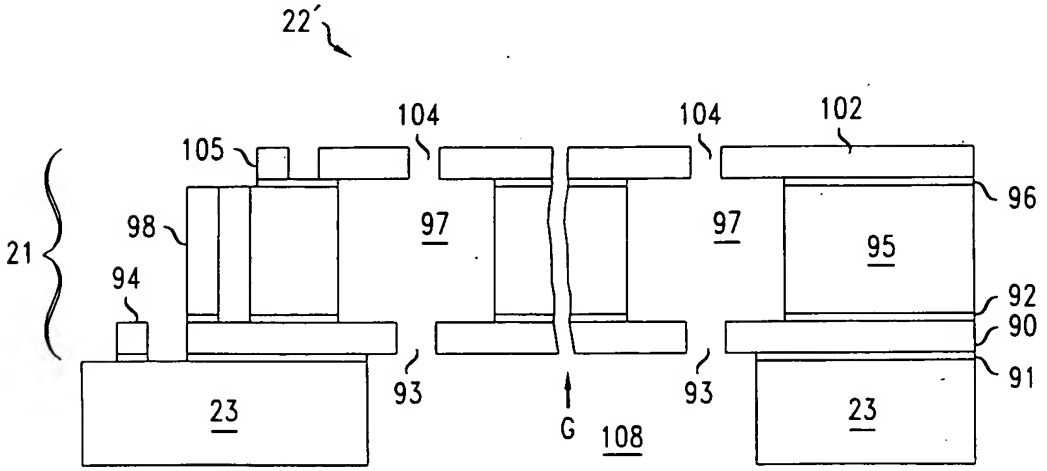
FIG. 13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